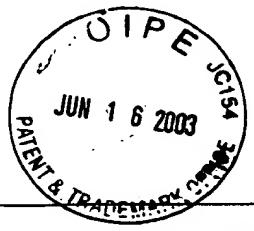
AF/2187



U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE

APPEAL BRIEF TRANSMITTAL	Docket Number: 10191/1333	Conf. No. 4178

Application Number	Filing Date	Examiner	Art Unit
09/527,424	March 17, 2000	Kimberly N. MCLEAN-MAYO	2187

Invention Title	Inventor
METHOD AND DEVICE FOR SECURING DATA WHEN ALTERING THE STORAGE CONTENTS OF CONTROL UNITS	Rolf KOHLER et al.

Address to:

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P.O. Box 1450
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Date: 6/13, 2003 Reg. No. 36,197

Signature: _____
Jong H. Lee

Further to the Notice of Appeal dated March 28, 2003 (filed at the PTO on April 2, 2003) for the above-referenced application, enclosed are three copies of an Appeal Brief. Accompanying the Appeal Brief is the Appendix to the Appeal Brief.

The Commissioner is hereby authorized to charge payment of the 37 C.F.R. § 1.17(c) appeal brief filing fee of $320.00, a one-month extension fee of **$110.00**, and any additional fees associated with this communication to the deposit account of **Kenyon & Kenyon**, deposit account number **11-0600**.

Dated: 6/13, 2003 By: _____ (by Reg. No. 36,197)
Richard L. Mayer (Reg. No. 22,490)

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KENYON & KENYON
One Broadway
New York, N.Y. 10004
(212) 908-6479 (telephone)
(212) 425-5288 (facsimile)
CUSTOMER NO. 26646
PATENT & TRADEMARK OFFICE

[10191/1333]

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BOARD OF PATENT APPEALS AND INTERFERENCES

Applicants	:	Rolf KOHLER et al.
Serial No.	:	09/527,424
Filing Date	:	March 17, 2000
For	:	METHOD AND DEVICE FOR SECURING DATA WHEN ALTERING THE STORAGE CONTENTS OF CONTROL UNITS
Examiner	:	Kimberly N. McLEAN MAYO
Art Unit	:	2187
Confirmation No.	:	4178

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Date: 6/13, 2003 Reg. No. 36,197

Signature: _____
Jong H. Lee

APPELLANTS' APPEAL BRIEF
UNDER 37 C.F.R. § 1.192

S I R :

Applicants filed a Notice of Appeal dated March 28, 2003 (filed at the PTO on April 2, 2003) appealing from the Final Office Action dated October 30, 2002, in which claims 1-32 of the above-identified application were finally rejected. This Brief is submitted by Applicants in support of their appeal.

I. REAL PARTY IN INTEREST

The above-identified Applicants and Robert Bosch GmbH of Stuttgart, Germany, are the real parties in interest.

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II. RELATED APPEALS AND INTERFERENCES

No appeal or interference which will directly affect, or be directly affected by, or have a bearing on the Board's decision in the pending appeal is known to exist to the undersigned attorney or is believed by the undersigned attorney to be known to exist to Applicants.

III. STATUS OF CLAIMS

Claims 1-32 are pending in this application. Applicants appealed from the final rejection of claims 1-32 made in the final Office Action mailed by the Patent Office on October 30, 2002. Of the claims presently on appeal, claims 1, 12, 24 and 27 are independent; claims 2-11, 29 and 30 are dependent on claim 1; claims 13-23, 31 and 32 depend on claim 12; claims 25-26 depend on claim 24; and claim 28 depends on claim 27. Applicants filed a Rule 116 Response dated December 19, 2002, and the Examiner indicated in the Advisory Actions mailed on January 13, 2003 and March 5, 2003 that the 35 U.S.C. §112 rejection has been overcome.

IV. STATUS OF AMENDMENTS

A Rule 116 Amendment (amending claims 1, 3, 4, 5, 7, 9, 11, 12, 14-17, 19, 21, 23, 24, 26 and 27) was mailed on December 19, 2002, subsequent to the final Office Action mailed on October 30, 2002. In the Supplemental Advisory Action mailed on March 5, 2003, the Examiner indicated that the Rule 116 Amendment will be entered.

V. SUMMARY OF THE INVENTION

The present invention relates to a method and an associated device for programming data in a memory of a computer, where data and/or programs in a computer memory, in particular a control unit in a motor vehicle, are altered. (P. 1, l. 2-4). The method and the associated device serve to secure the functionality of a control unit, for example, when an interruption or malfunction has occurred during erasing and/or programming. (P. 2, l. 22-23). To do so, when an

interruption or a reset occurs during erasing or programming, or when the device otherwise becomes de-energized, this is noted in a memory device, e.g., in the memory device to be programmed. (P. 2, l. 23-26). In addition, in programming, an identifier that identifies correct erasing and/or programming of the memory is entered into an area of the memory that is to be erased and/or programmed later, in particular an area that is to be erased and/or programmed last, and this identifier is altered before erasing or programming the data or programs in such a way that the program is not executed if programming is incomplete and/or the data is not used if data entry is not complete. (P. 2, l. 26 - p. 3, l. 1). Thus, an error in programming or erasing can be corrected after a possible data modification. (P. 3, l. 1-2).

Explicit deletion of data and/or programs before the erasing and/or programming that are part of the programming operation may be omitted, because simply making the identifier unidentifiable is sufficient to prevent processing of the memory contents, and thus the memory contents need not be erased. (P. 3, l. 8-11). In addition, the time and the cause of the malfunction can be stored with a flag, for example, in a memory because in a special embodiment, an application, in particular a control cannot be executed with an emergency control program but instead only a memory or its data and/or programs that have been correctly entered as intended can be read out or used for control. (P. 3, l. 14-17).

Figure 1 shows as an example a hardware arrangement for implementing the method presented here, i.e., a computer system 100 having a microprocessor 106 connected to additional elements by a line system 109, in particular a bus system. (P. 4, l. 2-6). Various memory devices 104, 105 and 108 may be present in the control unit, but only one programmable and/or erasable nonvolatile or refreshable memory, shown here in the form of element 104, is necessary to illustrate the present invention. (P. 4, l. 11-12 and 23-25). Block 107 represents possible peripheral components, i.e., interface elements for connecting external peripherals. (P. 4, l. 27-28). Programming may in turn be performed by insertion of a data carrier in control unit 100 itself or by using data from internal

memories such as non-erasable, non-volatile memory 108. (P. 4, l. 30 - p. 5, l. 2). In addition, an external programming unit 101, e.g., a second control unit or computer may also be provided for programming and entering data either serially over interface 102 or as a parallel connection over a possible bus system 103. (P. 5, l. 2-5).

Figure 2 shows in detail the erasable or programmable nonvolatile memory 104, which is divided into various areas 200 to 205, for example, and in addition, there is a cell or a memory section 206 in memory area 205. (P. 5, l. 13-15). The division into memory areas as proposed in Figure 2 is optional because when using an external programming device 101, for example, some of areas 200-205 may be omitted. (P. 5, l. 27-29). Programming of nonvolatile memory 104 usually takes place from the lower memory area to the upper, area 206 being programmed last. (P. 5, l. 29-30).

Figure 3 shows a data and/or program section, in particular a program identifier 300 in memory 104, e.g., in memory section 206 of program memory area 205, which is programmed late in the sequence of the programming operation, preferably being programmed last. (P. 6, l. 1-4). This program identifier 300 may be subdivided into various subsections 301-304, which may include, for example, a predetermined number of bit positions or a column of a predetermined length of letters and numbers or any characters. (P. 6, l. 4-6). Before or during the programming operation, at least one subsection, e.g., subsection 301, is selected as identifier K and stored for later checking. (P. 6, l. 6-8).

In an example embodiment, a data and/or program section that is easy to recover, such as program identifier 300, is selected as the basis for identifier K, so the subsection(s) functioning as the identifier can also be recovered easily. (P. 6, l. 15-17). Its precise position should also be known even after modification to permit checking of identifier K. (P. 6, l. 17-18).

Subsection 301, which was selected as identifier K, for example, may

include any six characters, for example, as long as it is unambiguous, in which case the precise position of this subsection in the data and/or programs need not be known precisely. (P. 6, l. 20-23). However, if the position of identifier K is known precisely as first subsection 301 of program identifier 300 and if the number of characters or bits is known precisely because it is predetermined, then it is possible to use an identifier K which occurs more frequently in the data and/or programs already programmed or to be programmed. (P. 6, l. 24-27).

Figure 4 shows a flow chart of how programming with safeguarding of a memory is performed in the case of nonvolatile memory 104, for example. (P. 7, l. 1-2). The safeguarding effect is achieved by the fact that before erasing or programming the entire memory or a block or a page, depending on the type of flash EPROM used, an identifier at the end of the last existing block or the last page or the last cell of the entire memory, said identifier having been entered previously, which identifies correct erasing and/or programming of the memory, is rendered invalid by a change, e.g., by being erased or reprogrammed, in particular it is rendered unidentifiable, e.g., for a comparison query or a search query. (P. 7, l. 8-13). Such an identifier K may be, for example, a code of multiple letters and numbers which is erased or written over with zeros, for example, and an existing part of the data and/or programs of the program identifier is used, for example, which means this identifier K need not be programmed separately. (P. 7, l. 13-16). Only when the entire programming operation or the erase and reprogramming operation is concluded and identifier K has been entered again is the program valid again. (P. 7, l. 16-18). If there is any interruption, a reset, or if the device otherwise becomes de-energized during erasing and/or programming, the altered identifier K is not entered again and thus the program is not valid and cannot be executed. (P. 7, l. 18-20).

The operation starts in block 400 in Figure 4, and the program to be processed is determined first in block 401. (P. 7, l. 29-30). This determination can be made by preselecting a program identifier 300 or by selecting a flag having one or more bit positions, and this preselection is then checked in queries 402, 403

and 404. (P. 8, l. 2-4). Then, in an example embodiment, identifier K and/or the respective subsection(s) may also be specified in block 401. (P. 8, l. 7-8). In block 402 a query is then issued to determine whether driving program 1 has been selected by the program identification or the selection of flags, in which case the system returns to block 405. (P. 8, l. 10-12). Then a reset is triggered in block 405, performing the necessary initialization for driving program 1 and establishing the communication connection. (P. 8, l. 12-14). If it is found in query 402 that driving program 1 has not been selected, then a check is made in query 403, for example, to determine whether there is a programming request. (P. 8, l. 14-16). If a boot program, e.g., boot program 1 is selected in query 403, this leads to block 410 where there is also a reset to the beginning (reset) and initialization depending on boot program 1 and establishment of communication. (P. 8, l. 24-26).

In block 411, the session of the programming mode of the programming device is then started. (P. 8, l. 26-27). Next in block 412 identifier K is altered, in particular rendered unidentifiable as part of the program, in particular as part of program identifier 300 to advantage. (P. 8, l. 27-28). Before the change in identifier K, the identifier K and a possible flag for interruption of the programming operation may be analyzed. (P. 8, l. 29-30). Likewise, identifier K may be selected or predetermined here immediately before the change in identifier K by control unit 100 or a programming unit 101. (P. 8, l. 30 - p. 9, l. 1). Then the actual erasing or programming operation takes place in block 413, erasing by pages, blocks, globally or by cells and/or reprogramming, as mentioned above, depending on the memory used. (P. 9, l. 3-5). At the end of the programming operation in block 413 and/or after an interruption, e.g., due to a disturbance, a reset and/or a de-energized state of control unit 100 or microprocessor 106 of the programming operation, the correctness of identifier K is checked in block 415. (P. 9, l. 5-8). If identifier K is not recognized as correct, there is a renewed entry into the interrupted boot program. (P. 9, l. 8-9). However, if identifier K is identified as correct, this leads to block 414, the end of the process. (P. 9, l. 11-12). Since identifier K is entered into an area that is programmed as late as possible, preferably last, such as memory area 206 of programming area 205 in Figure 2, a

correct identifier K is available again only when the programming operation has been finished completely and correctly. (P. 9, l. 14-17).

For security reasons, identifier K and optionally the flag for an interruption may also be checked and analyzed in principle at the start of an application program, in particular a driving program for a motor vehicle and optionally also at the beginning of a programming routine or a boot program, i.e., in queries 402, 403, 404, etc. (P. 9, l. 19-22). Then it is advantageously possible to enter into an application program only if the correct program has been selected and in addition identifier K and/or the flag for an interruption has been checked and recognized as correct. (P. 9, l. 22-24).

VI. ISSUES FOR REVIEW

The following issues are presented for review on appeal in this case:

A) Whether claims 1-6, 12-18 and 24-32 are unpatentable under 35 U.S.C. § 103(a) over U.S. Patent No. 5,930,826 to Lee et al. ("Lee").

C) Whether claims 7-11 and 19-23 are unpatentable under 35 U.S.C. § 103(a) over Lee in view of Japanese Patent No. 09161493 to Yousuke et al. ("Yousuke").

VII. GROUPING OF CLAIMS

For purposes of this appeal, all claims do not stand and fall together. For the rejection of claims 1-6, 12-18 and 24-32, Applicants will argue claims 1-6, 16, 17, 24-26 and 29-30 as one group, and claims 12-15, 18, 27-28 and 31-32 will be argued as another group. For the rejection of claims 7-11 and 19-23, claims 7, 18, 19 and 20 will be argued individually; claims 9-11 will be argued as a group; and claims 21-23 will be argued as another group.

VIII. ARGUMENTS

A. THE REJECTION OF CLAIMS 1-6, 12-18, and 24-32 UNDER 35 U.S.C. § 103(a)

Claims 1-6, 12-18 and 24-32 have been rejected under 35 U.S.C. §

103(a) as being unpatentable over U.S. Patent 5,930,826 to Lee et al. ("Lee"). Applicants respectfully request reversal of this rejection for the reasons stated below.

In rejecting a claim under 35 U.S.C. § 103(a), the Examiner bears the initial burden of presenting a prima facie case of obviousness. In re Rijckaert, 9 F.3d 1531, 1532, 28 U.S.P.Q.2d 1955, 1956 (Fed. Cir. 1993). To establish prima facie obviousness, three criteria must be satisfied. First, there must be some suggestion or motivation to modify or combine reference teachings. In re Fine, 837 F.2d 1071, 5 U.S.P.Q.2d 1596 (Fed. Cir. 1988). This teaching or suggestion to make the claimed combination must be found in the prior art and not based on the application disclosure. In re Vaeck, 947 F.2d 488, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991). Second, there must be a reasonable expectation of success. In re Merck & Co., Inc., 800 F.2d 1091, 231 U.S.P.Q. 375 (Fed. Cir. 1986). Third, the prior art reference(s) must teach or suggest all of the claim limitations. In re Royka, 490 F.2d 981, 180 U.S.P.Q. 580 (C.C.P.A. 1974). In addition, generalized assertions that it would have been obvious to modify the reference teachings do not properly support a § 103 rejection. See In re Jones, 21 U.S.P.Q.2d 1941 (Fed. Cir. 1992). Furthermore, even if a claim concerns a "technologically simple concept," there still must be some finding as to the "specific understanding or principle within the knowledge of a skilled artisan" that would motivate a person having no knowledge of the claimed subject matter to "make the combination in the manner claimed." In re Kotzab, 55 U.S.P.Q.2d 1313, 1318 (Fed. Cir. 2000).

Independent claims 1, 12, 24 and 27 recite an "identifier identifying a correct at least one of erasing and programming of the memory arrangement." The Examiner asserted the following argument in support of the final rejection:

> Regarding Applicants' argument that Lee does not teach providing an identifier identifying a correct erasing and/or programming of an area in memory arrangement, the Examiner disagrees. Lee teaches that the identifier(s) are protection bits which prevent the corresponding data from being erased, programmed or read incorrectly (C 2, L 42-48;C 3, L 40-64; C 4, L 1-48) and thus the identifier in Lee's system does identify a

> correct erasing and/or programming memory arrangement. When the erase and/or program bits of the identifier indicate an unprotected state, the corresponding data is correct erasing and/or programming memory arrangement. **The phrase "correct erasing and/or programming" is interpreted to mean an approved area to erase or program.** (10/30/02 Office Action, *emphasis added*).

In addition, in the Advisory Action mailed on March 5, 2003, the Examiner further argued that the terms "correct" and "erasing" are "standard terms, and thus can be given a standard/general meaning," i.e., "an approved area to erase or program." Applicants respectfully disagree with the Examiner's interpretation of the phrase "correct erasing and/or programming," for the following reasons.

During patent examination, the pending claims must be interpreted in a manner "***consistent with the specification***." MPEP 2111. Reading a claim ***in light of the specification***, to thereby interpret limitations explicitly recited in the claim, is a quite different thing from reading limitations of the specification into a claim, to thereby narrow the scope of the claim. MPEP 2111. In addition, the broadest reasonable interpretation of the claims must also be consistent with the interpretation that those skilled in the art would reach. MPEP 2111. Furthermore, "Applicant may be his or her own lexicographer as long as the meaning assigned to the term is not repugnant to the term's well known usage." MPEP 2111.01.

While the Examiner asserts that the "standard" meaning to be attributed to the claimed phrase "correct erasing and/or programming" is "an approved area to erase or program," this interpretation is completely unsupported. In fact, Applicants' asserted interpretation of "correct erasing and/or programming," i.e., ***an erasing and/or programming operation has been completed correctly***, is more intuitively obvious. In addition, the meaning of the phrase "correct erasing and/or programming" is clearly described throughout Specification to be consistent with the interpretation asserted by Applicants. For example, the Specification indicates the following:

> The method and the respective device serve to secure the functionality of a control unit, for example, when an

> interruption or malfunction has occurred during erasing and/or programming. To do so, when an interruption or a reset occurs during erasing or programming or when the device otherwise becomes de-energized, this is noted in a memory device, in particular in the memory device to be programmed. **In addition, in programming an identifier that identifies correct erasing and/or programming of the memory is entered into an area of the memory that is to be erased and/or programmed later**, in particular an area that is to be erased and/or programmed last, **and this identifier is altered before erasing or programming the data or programs in such a way that the program is not executed if programming is incomplete and/or the data is not used if data entry is not complete.** Thus, an error in programming or erasing can be corrected after a possible data modification.
>
> Advantageously, **the expected identifier that identifies the completeness and accuracy of the programming** is used as part of the program, in particular as part of the program identifier itself, and consequently does not take up any additional memory. (Specification, p. 3, l. 23 - p. 4, l. 6, *emphasis added*).

Thus, when viewed in light of the Specification, it is clear that the phrase "correct erasing and/or programming" as used in the present application means that an erasing and/or programming operation has been completed correctly, not "an approved area to erase or program" as asserted by the Examiner.

Lee describes PGM-bit, ERS-bit, and RD-bit, which are protection bits that prevent programming, erasing, and reading, respectively, of an area of memory when they are set. However, these bits do not indicate whether the respective operations were completed correctly. Therefore, Lee does not disclose or suggest an "identifier identifying a correct at least one of erasing and programming of the memory arrangement," as recited in claims1, 12, 24 and 27. For at least this reason, claims 1, 12, 24 and 27, as well as their dependent claims 2-6, 13-18, 25-26 and 28-32, are patentable over Lee.

Independent of the above, claims 1-6, 16, 17, 24-26 and 29-30 are patentable over Lee for the following additional reason. Claim 1 recites:

> A method of at least one of erasing and programming information in a memory arrangement of a computer, comprising the steps of:
>
> providing an identifier into an area of the memory arrangement that is to be at least one of erased and programmed, the identifier identifying a correct at least one of erasing and programming of the memory arrangement; and
>
> **altering the identifier in the memory arrangement before at least one of erasing and programming the information**.

Claim 24 is a device claim substantially corresponding to claim 1. Claim 16, which depends from claim 12, also recites "altering the selected identifier . . . before at least one of erasing and programming the information." Claim 17 depends from claim 16. While the Examiner asserts that one may use the protection bits disclosed in Lee as the identifier recited in Claim 1, such an attempt would prevent the system of Lee from operating properly. Lee states:

> The protection information of each memory sector is stored in the protection bit array 11. The protection bit array 11 comprises three bits of information, i.e., **ERS-bit 81, PGM-bit 82 and RD-bit 83, for indicating the protection state of erase, program, and read operations** respectively for each sector. The data of a sector are read to a memory sense amplifier 13, and the protection bits are read to a protection sense amplifier 14, respectively. Before any further operation on the data of the selected sector is executed, the corresponding protection bit is examined first. **If it shows that the selected sector is protected, the operation will be terminated**. (Lee, col. 3, ll. 50-64, *emphasis added*).

Thus, applying the argument asserted by the Examiner in the final Office Action, the following would result from applying Lee to Claim 1:

1) The PGM-bit would identify a correct programming of an area in memory. That is, when PGM-bit is set, the area is approved to be programmed and when not set, the area is not approved.
2) PGM-bit is set and provided into an area of memory identifying a correct programming the memory (approved for programming).
3) The PGM-bit is altered (cleared B not set) before programming or erasing the memory.

Since the PGM-bit only has two states, altering a set PGM-bit causes it to be cleared or not set. When the PGM-bit is not set, it indicates a protected state. Thus, according to Lee, subsequent attempt to program the area of memory would be terminated. (Lee, col. 3, ll. 50-64). Therefore, using the PGM-bit as the identifier recited in Claim 1 would prevent the system of Lee from being able to program the area of memory. The ERB-bit operates with the erase function in the same way as the PGM-bit does for the program function, and the erase function would likewise fail to operate according to Claim 1. Thus, using the protection bits described in Lee as the identifier recited in Claim 1 would render the system of Lee inoperable. If a proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. *In re Gordon*, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984). If the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie obvious*. *In re Ratti*, 270 F.2d 810, 123 USPQ 349 (CCPA 1959); M.P.E.P. §2143.01. Therefore, Lee fails to render obvious claims 1, 16, 17 and 24, as well as their dependent claims 2-6, 25-26 and 29-30.

For the foregoing reasons, applicants respectfully submit that claims 1-6, 12-18 and 24-32 are patentable over Lee. Therefore, it is respectfully requested that this rejection be withdrawn.

B. THE REJECTION OF CLAIMS 7-11 AND 19-23 UNDER 35 U.S.C. § 103(a)

Claims 7-11 and 19-23 stand rejected under 35 U.S.C. § 103 as being unpatentable over U.S. Patent 5,930,826 to Lee et al. ("Lee") in view of Japanese Patent 09161493 to Yousuke et al. ("Yousuke"). Applicants respectfully submit that this rejection should be reversed for the following reasons.

In rejecting a claim under 35 U.S.C. § 103(a), the Examiner bears the

initial burden of presenting a prima facie case of obviousness. In re Rijckaert, 9 F.3d 1531, 1532, 28 U.S.P.Q.2d 1955, 1956 (Fed. Cir. 1993). To establish prima facie obviousness, three criteria must be satisfied. First, there must be some suggestion or motivation to modify or combine reference teachings. In re Fine, 837 F.2d 1071, 5 U.S.P.Q.2d 1596 (Fed. Cir. 1988). This teaching or suggestion to make the claimed combination must be found in the prior art and not based on the application disclosure. In re Vaeck, 947 F.2d 488, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991). Second, there must be a reasonable expectation of success. In re Merck & Co., Inc., 800 F.2d 1091, 231 U.S.P.Q. 375 (Fed. Cir. 1986). Third, the prior art reference(s) must teach or suggest all of the claim limitations. In re Royka, 490 F.2d 981, 180 U.S.P.Q. 580 (C.C.P.A. 1974). In addition, generalized assertions that it would have been obvious to modify the reference teachings do not properly support a § 103 rejection. See In re Jones, 21 U.S.P.Q.2d 1941 (Fed. Cir. 1992). Furthermore, even if a claim concerns a "technologically simple concept," there still must be some finding as to the "specific understanding or principle within the knowledge of a skilled artisan" that would motivate a person having no knowledge of the claimed subject matter to "make the combination in the manner claimed." In re Kotzab, 55 U.S.P.Q.2d 1313, 1318 (Fed. Cir. 2000).

During patent examination, the pending claims must be interpreted in a manner "***consistent with the specification.***" MPEP 2111. Reading a claim ***in light of the specification***, to thereby interpret limitations explicitly recited in the claim, is a quite different thing from reading limitations of the specification into a claim, to thereby narrow the scope of the claim. MPEP 2111. In addition, the broadest reasonable interpretation of the claims must also be consistent with the interpretation that those skilled in the art would reach. MPEP 2111. Furthermore, "Applicant may be his or her own lexicographer as long as the meaning assigned to the term is not repugnant to the term's well known usage." MPEP 2111.01.

Claims 7-11 ultimately depend on claim 1, and claims 19-23 ultimately depend on claim 12. As discussed above in detail in connection with the rejection of claims 1 and 12, Lee does not disclose an "identifier identifying a correct at least

one of erasing and programming of the memory arrangement." Furthermore, the Yousuke reference also fails to disclose or suggest this limitation. According to the Examiner, "Yousuke is not provided in the rejection to suggest modifying Lee to include an identifier identifying a correct erasing and/or programming area of memory arrangement as this feature is already taught by Lee." (10/30/02 Final Office Action). Since the Yousuke reference is not cited for, and does not suggest, modifying Lee to include an identifier identifying a correct erasing and/or programming area of memory arrangement as recited in claims 1 and 12, the combination of Lee and Yousuke does not render obvious dependent claims 7-11 and 19-23.

Independent of the above, further regarding claims 7-11, which depend on claim 1 reciting "**altering the identifier in the memory arrangement before at least one of erasing and programming the information**," using the protection bits disclosed in Lee as the identifier recited in Claim 1, as asserted by the Examiner, would prevent the system of Lee from operating properly, for the reasons explained above in detail in connection with the rejection of claim 1. If a proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. *In re Gordon*, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984). If the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie obvious*. *In re Ratti*, 270 F.2d 810, 123 USPQ 349 (CCPA 1959); M.P.E.P. §2143.01. Therefore, the combination of Lee and Yousuke fails to render obvious claims 7-11 dependent on claim 1.

Independent of the above, with specific regard to claims 7 and 19, Applicants point out that Lee also fails to describe the *altering* of an identifier in a memory arrangement so that the identifier is *unidentifiable*, as the Examiner has conceded in the final Office Action. Rather, Lee teaches the use of protection bits, which are either set or not set, and are therefore *identifiable* after alteration.

Yousuke sets a write execution display flag before the write operation, and if the write operation is successful, the write execution display flag is replaced with a write end display flag. Indeed, the flags disclosed in Yousuke are quite similar to the bits disclosed in Lee, and thus both flags are identifiable, contrary to the Examiner's assertion. For at least this additional reason, claims 7 and 19 are not rendered obvious by the combination of Lee and Yousuke.

Independent of the above, with specific regard to claims 8 and 20, Lee fails to describe an identifier being a section of a program identifier, as the Examiner has conceded in the final Office Action. Rather, Lee teaches the use of separate protection bits, as discussed above. While the Examiner relies on Yousuke to provide a program identifier, Applicants respectfully assert that the display flags of Yousuke are not program identifiers as claimed. Indeed, Yousuke makes no mention of program identifiers. For at least this additional reason, claims 8 and 20 are not rendered obvious by the combination of Lee and Yousuke.

For at least the above reasons, claims 7-11 and 19-23 are allowable over Lee and Yousuke. Accordingly, reversal of the rejection of claims 7-11 and 19-23 is requested.

IX. CONCLUSION

For the foregoing reasons, it is respectfully submitted that the final rejection of claims 1-32 should be reversed.

Respectfully submitted,

KENYON & KENYON

Dated: 6/13, 2003

By: [signature] (by [signature] Reg. No. 36,157)

Richard L. Mayer
Reg. No. 22,490

CUSTOMER NO. 26646
PATENT TRADEMARK OFFICE

[10191/1333]

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BOARD OF PATENT APPEALS AND INTERFERENCES

Applicants	:	Rolf KOHLER et al.
Serial No.	:	09/527,424
Filed	:	March 17, 2000
For	:	METHOD AND DEVICE FOR SECURING DATA WHEN ALTERING THE STORAGE CONTENTS OF CONTROL UNITS
Examiner	:	Kimberly N. McCLEAN-MAYO
Art Unit	:	2187
Confirmation No.	:	4178

Mail Stop Appeal Brief-Patents
Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

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Date: 6/13, 2003 Reg. No. 36,197

Signature: _____
Jong H. Lee

APPENDIX TO APPELLANTS' APPEAL BRIEF
UNDER 37 C.F.R. § 1.192

S I R :

The claims involved in this appeal, claims 1-32, in their current form after entry of all amendments presented during the course of prosecution, are set forth below:

APPEALED CLAIMS:

1. A method of at least one of erasing and programming information in a

memory arrangement of a computer, comprising the steps of:

providing an identifier into an area of the memory arrangement that is to be at least one of erased and programmed, the identifier identifying a correct at least one of erasing and programming of the memory arrangement; and

altering the identifier in the memory arrangement before at least one of erasing and programming the information.

2. The method according to Claim 1, wherein the computer is a control unit in a motor vehicle.

3. The method according to Claim 1, wherein the altering step includes the substep of:

altering the identifier by at least one of erasing and programming.

4. The method according to Claim 1, further comprising the step of:

entering the identifier into a further area of the memory arrangement, the further area being at least one of erased and programmed only after at least one of erasing and programming of the area.

5. The method according to Claim 4, wherein the further area is to be at least one of erased and programmed last.

6. The method according to claim 1, wherein the identifier is a component of the information.

7. The method according to Claim 1, further comprising the step of:

altering the identifier by at least one of erasing and programming so that the identifier is unidentifiable.

8. The method according to claim 1, wherein the identifier is a section of a program identifier which identifies the respective information.

9. The method according to Claim 1, further comprising the step of:

checking the identifier after at least one of (a) an interruption in at least one of erasing and programming and (b) at least one of erasing and programming the memory arrangement.

10. The method according to Claim 9, further comprising the step of:

storing the interruption with a flag in the memory arrangement.

11. The method according to Claim 10, further comprising the steps of:

checking at least one of the identifier and the flag before at least one of erasing and programming; and

analyzing at least one of the identifier and the flag before at least one of erasing and programming.

12. A method of reprogramming information in a memory arrangement of a computer, comprising the step of:

selecting an identifier from the information entered into an area of the

memory to be at least one of erased and programmed, the identifier identifying a correct at least one of erasing and programming of the memory arrangement.

13. The method according to Claim 12, wherein the computer is a control unit in a motor vehicle.

14. The method according to claim 12, further comprising the step of:

selecting the identifier from the information entered into a further area of the memory arrangement, the further area being at least one of erased and programmed only after at least one of erasing and programming of the area.

15. The method according to Claim 14, wherein the further area is to be at least one of erased and programmed last.

16. The method according to claim 12, further comprising the step of:

altering the selected identifier in the memory arrangement before at least one of erasing and programming the information.

17. The method according to Claim 16, wherein the altering step includes the substep of:

altering the selected identifier by at least one of erasing and programming.

18. The method according to claim 12, further comprising the step of:

selecting the identifier as at least one section of a predetermined length of

the information entered into the memory arrangement.

19. The method according to Claim 12, further comprising the step of:

altering the identifier by at least one of erasing and programming so that the identifier is unidentifiable.

20. The method according to claim 12, wherein the identifier is a section of a program identifier which identifies the information.

21. The method according to Claim 12, further comprising the step of:

checking the identifier after at least one of (a) an interruption in at least one of erasing and programming and (b) at least one of erasing and programming the memory arrangement.

22. The method according to Claim 21, further comprising the step of:

storing the interruption with a flag in the memory arrangement.

23. The method according to Claim 22, further comprising the steps of:

checking at least one of the identifier and the flag before at least one of erasing and programming; and

analyzing at least one of the identifier and the flag before at least one of erasing and programming.

24. A device for at least one of erasing and programming information in a memory arrangement of a computer, comprising:

a programming arrangement entering an identifier into an area of the memory arrangement to be at least one of erased and programmed, the identifier identifying a correct at least one of erasing and programming of the memory arrangement, the programming arrangement altering the identifier in the memory arrangement before at least one of erasing and programming the information.

25. The device according to Claim 24, wherein the computer is a control unit in a motor vehicle.

26. The device according to Claim 24, wherein the identifier is altered by at least one of erasing and programming.

27. A device, comprising:

a reprogramming arrangement reprogramming information in a memory arrangement of a computer, the reprogramming arrangement selecting an identifier from the information entered into an area of the memory arrangement to be at least one of erased and programmed, the identifier identifying a correct at least one of erasing and programming of the memory arrangement.

28. The device according to Claim 27, wherein the computer is a control unit in a motor vehicle.

29. The method of claim 1 wherein the information includes data.

30. The method of claim 1 wherein the information includes programs.

31. The method of claim 12 wherein the information includes data.

32. The method of claim 12 wherein the information includes programs.

Respectfully submitted,

KENYON & KENYON

Dated: 6/13, 2003

By: for Richard Mayer (by Reg. No. 36,197)
Richard L. Mayer
Reg. No. 22,490

CUSTOMER NO. 26646
PATENT & TRADEMARK OFFICE